

What is claimed is:

1. A memory device comprising:
  - a semiconductor substrate;
  - an NPN-type transistor formed on the semiconductor substrate;
  - an interlayer insulating film formed on the semiconductor substrate to cover the transistor, in which a contact hole exposing a source region of the transistor is formed;
  - a conductive plug filling the contact hole;
  - a resistant material in which a bit data "0" or "1" is to be written formed on the conductive plug; and
  - a conductive plate formed on the interlayer insulating film to be contacted with the resistant material.
2. The memory device as claimed in claim 1 further comprising a first material film through which electrons can tunnel, positioned between the conductive plug and the resistant material.
3. The memory device as claimed in claim 1, further comprising a second material film through which electrons can tunnel, positioned between the resistant material and the conductive plate.

4. The memory device as claimed in claim 2, further comprising a second material film through which electrons can tunnel, positioned between the resistant material and the conductive plate.

5. The memory device as claimed in claim 2, wherein the first material film is an n-type poly silicon film, a p-type poly silicon film, a silicon oxide film or an aluminum oxide film.

6. The memory device as claimed in claim 3, wherein the second material film is an n-type poly silicon film, a p-type poly silicon film, a silicon oxide film or an aluminum oxide film.

7. The memory device as claimed in claim 4, wherein the second material film is an n-type poly silicon film, a p-type poly silicon film, a silicon oxide film or an aluminum oxide film.

8. The memory device as claimed in claim 1, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

9. The memory device as claimed in claim 2, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

10. The memory device as claimed in claim 8, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

11. The memory device as claimed in claim 9, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

12. The memory device as claimed in claim 10, wherein when the resistant material is the silicon nitride film, the conductive plug is the same material layer as the material layer of the source region and the conductive plate is an aluminum (Al) plate.

13. The memory device as claimed in claim 11, wherein when the resistant material is the silicon nitride film, the conductive plug is the same material layer as the material layer of the source region and the conductive plate is an aluminum (Al) plate.

14. The memory device as claimed in claim 10, wherein when the resistant material is the aluminum oxide film, the conductive plug is a gold (Au) plug or a platinum (Pt) plug, and the conductive plate is an aluminum (Al) plate.

15. The memory device as claimed in claim 11, wherein when the resistant material is the aluminum oxide film, the conductive plug is a gold (Au) plug or a platinum (Pt) plug, and the conductive plate is an aluminum (Al) plate.

16. The memory device as claimed in claim 3, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

17. The memory device as claimed in claim 4, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

18. The memory device as claimed in claim 16, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

19. The memory device as claimed in claim 17, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

20. The memory device as claimed in claim 18, wherein when the resistant material is the silicon nitride film, the conductive plug is the same material layer as the material layer of the source region and the conductive plate is an aluminum (Al) plate.

21. The memory device as claimed in claim 19, wherein when the resistant material is the silicon nitride film, the conductive plug is the same material layer as the material layer of the source region and the conductive plate is an aluminum (Al) plate.

22. The memory device as claimed in claim 18, wherein when the resistant material is the aluminum oxide film, the conductive plug is a gold (Au) plug or a platinum (Pt) plug, and the conductive plate is an aluminum (Al) plate.

23. The memory device as claimed in claim 19, wherein when the resistant material is the aluminum oxide film, the conductive plug is a gold (Au) plug or a platinum (Pt) plug, and the conductive plate is an aluminum (Al) plate.

24. The memory device as claimed in claim 1, wherein a material layer consisting of the conductive plug, the resistant material and the conductive plate has a thickness such that charges used for writing the bit data can tunnel through the material layer.

25. The memory device as claimed in claim 2, wherein a material layer consisting of the conductive plug, the first material film, the resistant material and the conductive plate has a thickness such that charges used for writing the bit data can tunnel through the material layer.

26. The memory device as claimed in claim 3, wherein a material layer consisting of the conductive plug, the first material film, the resistant material, the second material film and the conductive plate has a thickness such that charges used for writing the bit data can tunnel through the material layer.

27. The memory device as claimed in claim 3, wherein a material layer consisting of the conductive plug, the first material film, the resistant material, the second material film and the conductive plate has a thickness such that charges used for writing the bit data can tunnel through the material layer.

28. The memory device as claimed in claim 1, wherein the resistant material is formed of a plurality of amorphous dielectric films.

29. A memory device comprising:
  - a semiconductor substrate;
  - an NPN-type transistor formed on the semiconductor substrate;
  - an interlayer insulating film formed on the semiconductor substrate to cover the transistor, in which a contact hole exposing a source region of the transistor is formed;
  - an insulating film formed on the entire surface of the source region exposed through the contact hole;
  - a resistant material in which a bit data "0" or "1" is written formed on the interlayer insulating film to be contacted with the entire surface of the insulating film; and
  - a conductive plate covering the entire surface of the resistant material.
30. The memory device as claimed in claim 29 further comprising a material film through which electrons can tunnel, positioned between the resistant material and the conductive plate.
31. The memory device as claimed in claim 29, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

32. The memory device as claimed in claim 30, wherein the resistant material is an amorphous dielectric film capable of trapping electrons during a predetermined time required for storing data according to predetermined values or directions of a voltage or current.

33. The memory device as claimed in claim 31, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

34. The memory device as claimed in claim 32, wherein the amorphous dielectric film is a silicon nitride film ( $\text{Si}_3\text{N}_4$ ) or an aluminum oxide film ( $\text{Al}_2\text{O}_3$ ).

35. The memory device as claimed in claim 33, wherein when the resistant material is the silicon nitride film, the conductive plate is an aluminum (Al) plate.

36. The memory device as claimed in claim 34, wherein when the resistant material is the silicon nitride film, the conductive plate is an aluminum (Al) plate.

37. The memory device as claimed in claim 33, wherein when the resistant material is the aluminum oxide film, the conductive plate is an aluminum (Al) plate.

38. The memory device as claimed in claim 34, wherein when the resistant material is the aluminum oxide film, the conductive plate is an aluminum (Al) plate.

39. The memory device as claimed in claim 30, wherein the material film is an n-type poly silicon film, a p-type poly silicon film, a silicon oxide film or an aluminum oxide film.

40. A method for writing bit data of a memory device that includes a semiconductor substrate; an NPN-type transistor formed on the semiconductor substrate; an interlayer insulating film formed on the semiconductor substrate to cover the transistor, in which a contact hole exposing a source region of the transistor is formed; a conductive plug filling the contact hole; a resistant material in which a bit data "0" or "1" is written formed on the conductive plug; and a conductive plate formed on the interlayer insulating film to be contacted with the resistant material, the method comprising:

initializing the resistant material; and

charging the resistant material to write the bit data "0" or "1" therein.

41. The method as claimed in claim 40, wherein the conductivity of the resistant material is enhanced by a forming process.

42. The method as claimed in claim 41, wherein a forming voltage is applied to a drain region of the transistor.

43. The method as claimed in claim 40, wherein the transistor is on, a bit line voltage ( $V_b$ ) is applied to a drain region of the transistor and a plate voltage ( $V_b/2$ ) is applied to the conductive plate, to write the bit data "0" or "1" in the resistant material.

44. The method as claimed in claim 43, wherein after the bit data "0" or "1" is written, the transistor is turned off to lengthen a retaining time of the bit data.

45. A method for writing bit data of a memory device that includes a semiconductor substrate; an NPN-type transistor formed on the semiconductor substrate; an interlayer insulating film formed on the semiconductor substrate to cover the transistor, in which a contact hole exposing the source region of the transistor is formed; a conductive plug filling the contact hole; a resistant material in which a bit data "0" or "1" is written formed on the conductive plug;

and a conductive plate formed on the interlayer insulating film to be contacted with the resistant material, the method comprising:

initializing the resistant material; and  
enhancing the resistance of the resistant material and writing the bit data "0" or "1" therein.

46. The method as claimed in claim 45, wherein a conductivity of the resistant material is enhanced by a forming process.

47. The method as claimed in claim 46, wherein a forming voltage is applied to a drain region of the transistor.

48. The method as claimed in claim 45, wherein the resistant material is discharged to enhance the resistance of the resistant material.

49. The method as claimed in claim 48, wherein the transistor is turned on and a plate voltage ( $V_b/2$ ) is applied to the conductive plate, to enhance the resistance of the resistant material.

50. The method as claimed in claim 45, wherein the transistor is turned on and a switching voltage ( $V_s$ ) is applied to the conductive plate, to enhance the resistance of the resistant material.

51. The method as claimed in claim 45, wherein the resistant material, as an amorphous dielectric film, is a silicon nitride film or an aluminum oxide film.

52. The method as claimed in claim 51, wherein when the resistant material is the silicon nitride film, the transistor is turned on, an opposite voltage to a bit line voltage ( $V_b$ ) is applied to a drain region of the transistor and a plate voltage ( $V_b/2$ ) is applied to the conductive plate, to enhance the resistance of the resistant material.

53. The method as claimed in claim 51, wherein when the resistant material is the aluminum oxide film, the transistor is turned on, a different voltage from a bit line voltage ( $V_b$ ) is applied to a drain region of the transistor and a plate voltage ( $V_b/2$ ) is applied to the conductive plate, to enhance the resistance of the resistant material.

54. A method for reading a written bit data in a memory device that includes a semiconductor substrate; an NPN-type transistor formed on the semiconductor substrate; an interlayer insulating film formed on the semiconductor substrate to cover the transistor, in which a contact hole exposing a source region of the transistor is formed; a conductive plug filling the contact hole; a resistant material in which a bit data "0" or "1" is written formed

on the conductive plug; and a conductive plate formed on the interlayer insulating film to be contacted with the resistant material, wherein the bit data which is written in the resistant material is read by measuring a current flowing through the resistant material and reading the written bit data in the resistant material.

55. The method as claimed in claim 54, wherein after a sense amplifier is connected to a drain region of the transistor, the transistor is turned on and a reading voltage ( $V_r$ ) is applied to the conductive plate to measure the current flowing through the resistant material.